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SpringCard E663

Hardware integration guide

PRELIMINARY

www.springcard.com

Document Identification

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Abstract			

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Revision History

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1. Introduction

1.1. Abstract

SpringCard E663 is an OEM RFID and NFC reader module designed to be operated through the network. **SpringCard E663** embedds a complete Ethernet 10/100 stack (MAC & PHY) and supports the TCP/IP protocol stock (IPv4).

This document provides all necessary information to integrate the **E663** OEM module into your design, and take benefit from all its features.

1.2. Product identification

1.2.1. Hardware

To date, only one hardware version of the **E663** OEM module exist:

- **E663S** ' output is balanced (symmetrical) so it could drive a **directly-matched, balanced antenna**. The distance between the module and the antenna shall not exceed 20cm.

1.2.2. Related products

SpringCard E663 is the core of two wall-mount access control readers:

- **SpringCard FynkyGate-IP NFC**, brinding TCP/IP up to the gate,
- **SpringCard FynkyGate-IP+POE NFC**, same as above with Power Over Ethernet feature.

1.3. Related documents

Editor	Doc #	Description
SpringCard	PMA13257	FunkyGate-IP NFC Integration and Configuration Guide

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1.4. Important – read me first

1.4.1. Antenna design

The **E663** OEM module needs an external antenna to work as a contactless (RFID / NFC) coupler. The antenna has to be designed carefully for the target module (balanced, symmetrical antenna for **H663S**) and depending on your own specifications (size constraints, expected operating distance), but flexibility is limited to some extent due to the requirements of the ISO standards and the EMC regulations.

SpringCard engineers have a strong experience in antenna design. Do not hesitate to consult us any time you need a custom design.

We also offer a **ready-to-use reader**, featuring the **E663** module mounted on an antenna; please visit www.springcard.com and look for the **FunkyGate** family.

1.5. Audience

This manual is designed for use by electronic hardware integrators. It assumes that the reader has expert knowledge of digital electronics.

1.6. Support and updates

Related documentation (e.g. product datasheets, application notes, sample software, HOWTOs and FAQs…) is available at SpringCard's web site:

www.springcard.com

Updated versions of this document and others are posted on this web site as soon as they are available.

For technical support enquiries, please refer to SpringCard support page, on the web at

www.springcard.com/support

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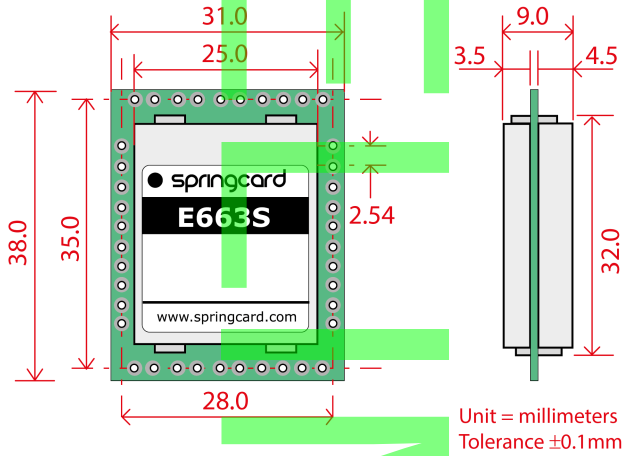
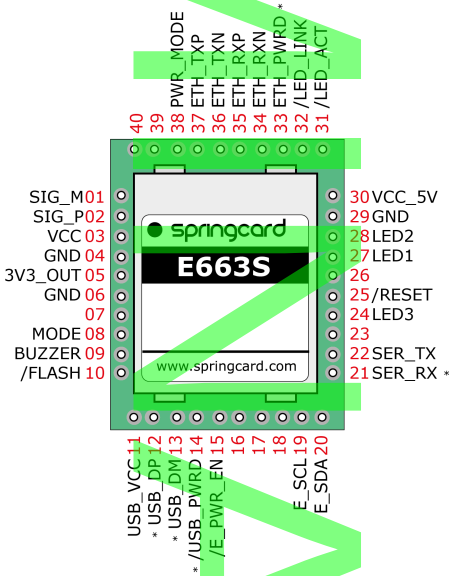
2. Hardware and pinout - E663S

2.1. Dimensions



2.2. Pinout



*NB: the **E663**'s main power supply is 5V DC (VCC_5V), but its core CPU operates at 3.3V. In the drawing above, the asterisk (*) denotes a 3.3V-only input pin (where the other input pins are 5V tolerant).*

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Table 2: pinout details for H663S

PIN	NAME	Type	Description	Remark	See §
1	SIG_M	Analog	Symmetric antenna		5.1
2	SIG_P	Analog	Symmetric antenna		5.1
3	VCC	Power	Power supply		4.1.2
4	GND	Ground	Ground		
5	3V3_OUT	Power Out	3.3V output	Max 100mA	
6	GND	Ground	Ground		
7			*RFU*	Leave unconnected	
8	MODE	IN	Firmware upgrade mode	Internal pull-up to VCC	4.7
9	BUZZER	OUT	Buzzer output		4.4
10	/FLASH	IN	Firmware upgrade	Internal pull-up to VCC	4.7
11	USB_VCC	Power	Bus power supply for USB link		4.6
12	USB_DP	IN/OUT	USB D+		4.6
13	USB_DM	IN/OUT	USB D-		4.6
14	/USB_PWRD	IN	E663 is powered by the bus	Internal pull-up to 3V3	4.6.2
15	/E_PWR_EN	OUT	Peripherals power management		
16			*RFU*	Leave unconnected	
17			*RFU*	Leave unconnected	
18			*RFU*	Leave unconnected	
19	E_SC_SCL	IN/OUT	I^2C SCL	Internal pull-up (10kΩ) to VCC	
20	E_SC_SDA	IN/OUT	I^2C SDA	Internal pull-up (10kΩ) to VCC	
21	SER_RX	IN	Serial port – host to E663	Internal pull-up (4.7kΩ) to 3V3	4.5
22	SER_TX	OUT	Serial port – E663 to host		4.5
23			*RFU*	Leave unconnected	
24	/LED3	OUT	LED 3	*BLUE*	4.3
25	/RESET	IN	E663 reset	Internal pull-up to VCC	4.1.3
26			*RFU*	Leave unconnected	

Table continuing next page

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Table 2 (continuing)

PIN	NAME	Type	Description	Remark	See §
27	/LED1	OUT	LED 1	*RED*	4.3
28	/LED2	OUT	LED 2	*GREEN*	4.3
29	GND	Ground	Ground		
30	VCC	Power	Power supply		4.1.2
31	/LED_ACT	OUT	Ethernet Activity LED		4.2
32	/LED_LINK	OUT	Ethernet Link LED		4.2
33	ETH_PWRD	IN	E663 is powered by a POE supply	Internal pull-up to 3V3	
34	ETH_RXN	IN	To RJ45		4.2
35	ETH_RXP	IN	To RJ45		4.2
36	ETH_TXN	OUT	To RJ45		4.2
37	ETH_TXP	OUT	To RJ45		4.2
38	PWR_MODE	OUT	E663 is in low power mode		
39			*RFU*	Leave unconnected	
40			*RFU*	Leave unconnected	

NB: for correct operation, all VCC pins (#3, #30) shall be connected to power supply, and all GND pins (#4, #6, #29) shall be connected to ground.

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3. Electrical characteristics

3.1. Absolute maximum ratings

Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	Parameter	Min	Max	Unit
VCC_{ABS}	DC supply voltage with respect to ground	-0.3	6.0	V
$V_{IN5,ABS}$ Pins 8, 10, 11, 19, 20, 25	Voltage to any pin with respect to ground 5V-tolerant input pins	-0.3	VCC+0.3	V
$V_{IN3,ABS}$ Pins 12, 13, 14, 21, 33	Voltage to any pin with respect to ground 3.3V-only input pins	-0.3	3,6	V
$I_{OUT,ABS}$	Total DC output current on all I/O pins		200	mA
$I_{SIGNAL\ PEAK}$	Peak current delivered by the SIGNAL pin		200	mA
$T_{STORAGE}$	Storage temperature	-20	+70	°C

3.2. Operating condition range

SYMBOL	Parameter	Condition	Min	Typ	Max	Unit
$T_{OPERATION}$	Operating temperature		-20	+25	+70	°C
VCC	Supply voltage		4.5	5.0	5.5	V
ICC	Power supply current	VCC = 5.0V		150	250	mA

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3.3. Input pin characteristics

Pins /RESET and /FLASH have 5V TTL input characteristics.

SYMBOL	Parameter	Min	Max	Unit
V_{IL}	LOW-level going threshold		0.8	V
V_{IH}	HIGH-level going threshold	2.0		V
I_{LEAK}	Input leakage current		4	µA

3.4. Output pin characteristics

Pins TX and /LEDx have TTL output characteristics.

SYMBOL	Parameter	Min	Max	Unit
V_{OL}	Output LOW-level		0.4	V
V_{OH}	Output HIGH-level	2.4		V
I_O	Output current source or sink		4	mA

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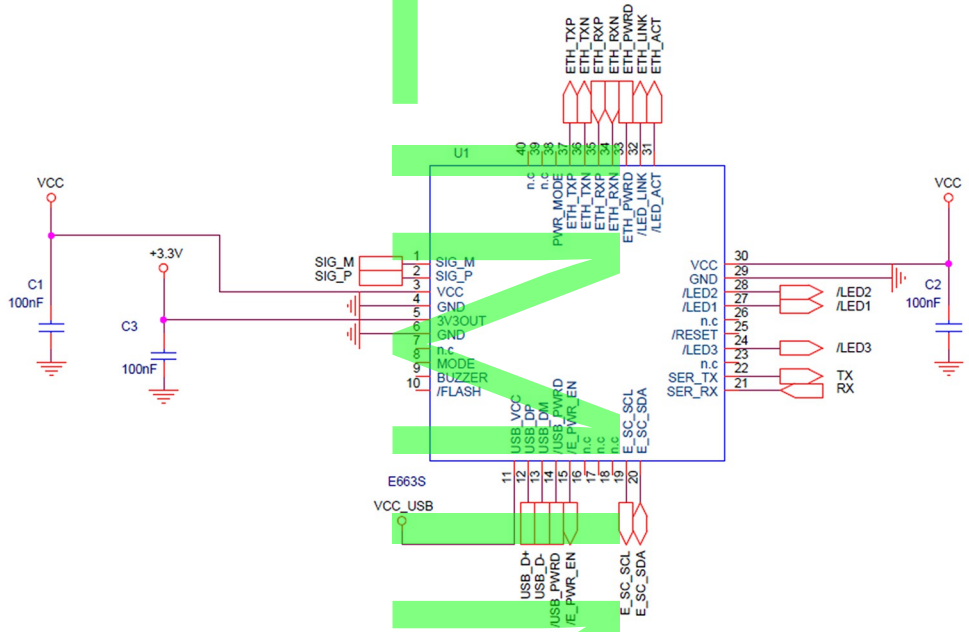
4. Integration guide

4.1. General

4.1.1. Minimal schematics

This is the minimal schematics to integrate the E663S in your design:



Decoupling capacitors C1, C2 and C3 shall be placed as closed as possible to the **E663** module.

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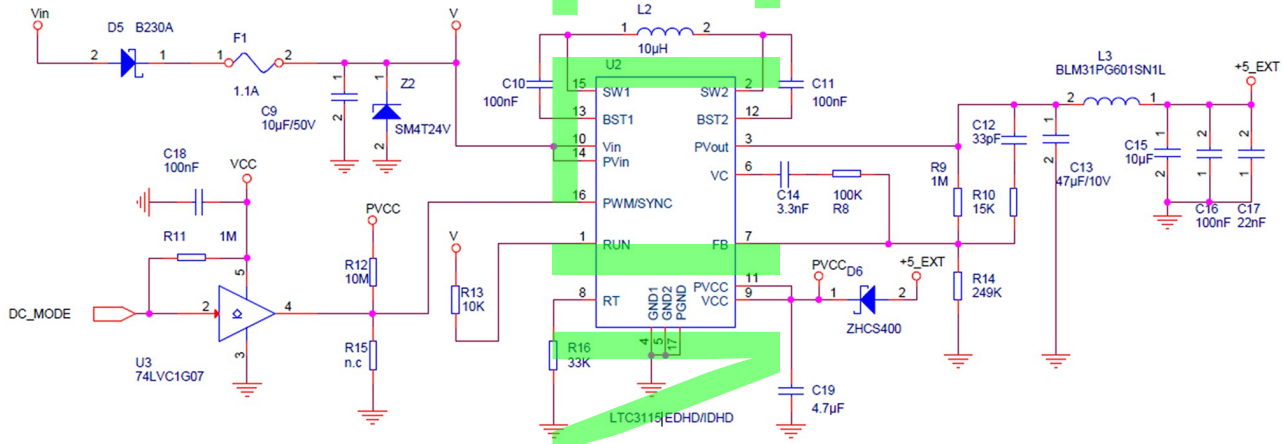
4.1.2. Power supply

SpringCard recommends to use a DC/DC converter to provide a clean VCC to the **E663**. A noisy or unstable VCC is the primary cause for reduced operating distance or communication errors.

Observe the following schematics, based on a LTC3115 chip. The **E663**'s PWR_MODE output pin (#33) is dedicated to drive the LTC3115 either in low current or high current mode (for reduced overall consumption).



4.1.3. Reset

The **E663** has its own reset supervisor. The /RESET pin (#25) shall be used only if a manual reset is needed. Otherwise, cycling the power is enough to ensure a proper reset of the module.

Tip: if you don't have to be able to reset the module externally, you may leave the /RESET pin unconnected.

When /RESET is set to LOW, the **E663**'s CPU stops. When /RESET is set to HIGH again, firmware execution restarts. Depending on the firmware release and the activated options, the **E663** needs 50 to 250ms to be ready after a reset.

Note that the /RESET pin has no effect on the RF front-end. If the RF field was ON before reset, it remains ON until the firmware instructs it to go OFF, or the module is powered down.

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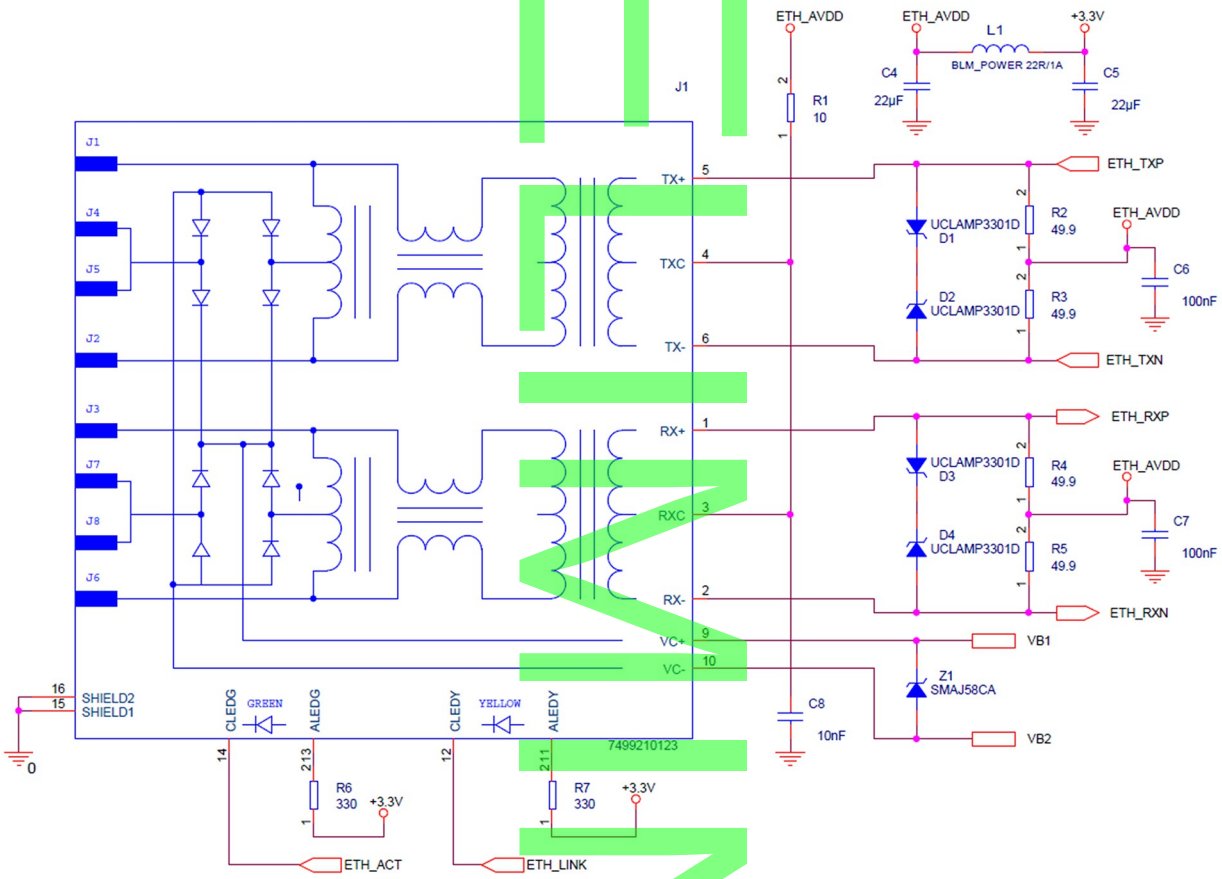
4.2. Ethernet

4.2.1. Connecting the E663 to a standard RJ45 socket



4.2.2. Behaviour of the Ethernet LEDs

[To be written]

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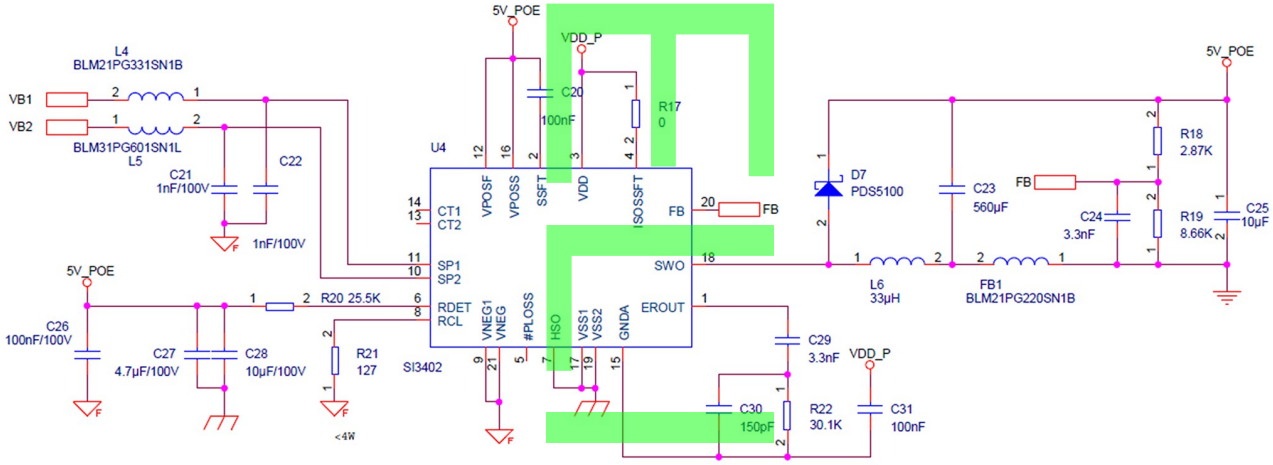
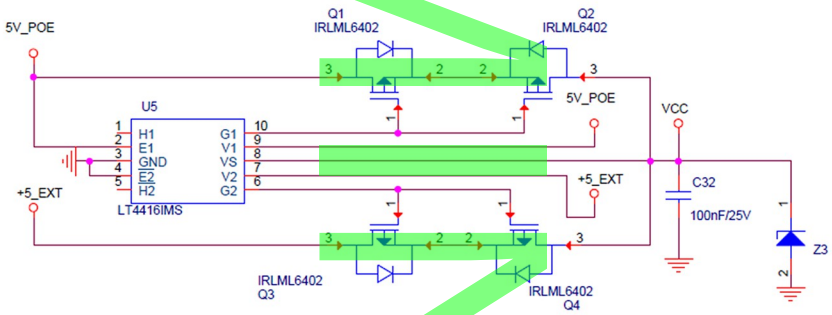
4.2.3. Power Over Ethernet (POE)

To implement the POE feature, SpringCard recommends the **SI3402** chip.



If you want your device to support both POE and external-power mode, use a **LTC4416** chip to select automatically between the two power sources.



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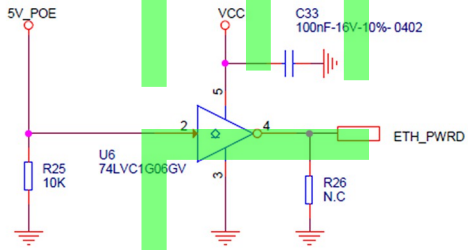
4.2.4. Powered by the POE, or external power

The ETH_PWRD pin (#33) tells the firmware whether the **E663** has an external power supply (LOW) or is powered by the POE (HIGH).

The schematics below shows how to inform the **E663** what the primary power source is.



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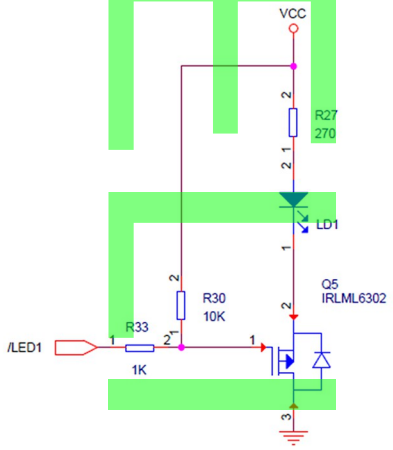
4.3. LED drivers

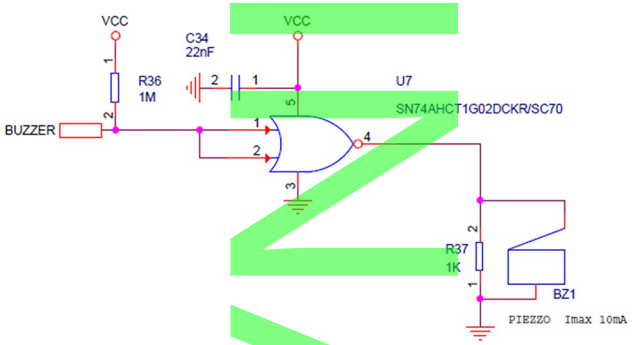
E663's LED output pins are active LOW and must be buffered to drive the LEDs.

Use N-channel mosfet transistors, as follow:



4.4. Buzzer

E663's BUZZER output pin is intended to drive a Piezo buzzer through a driver. To make the buzzer sound, a square wave at approx. 4.1kHz is generated.



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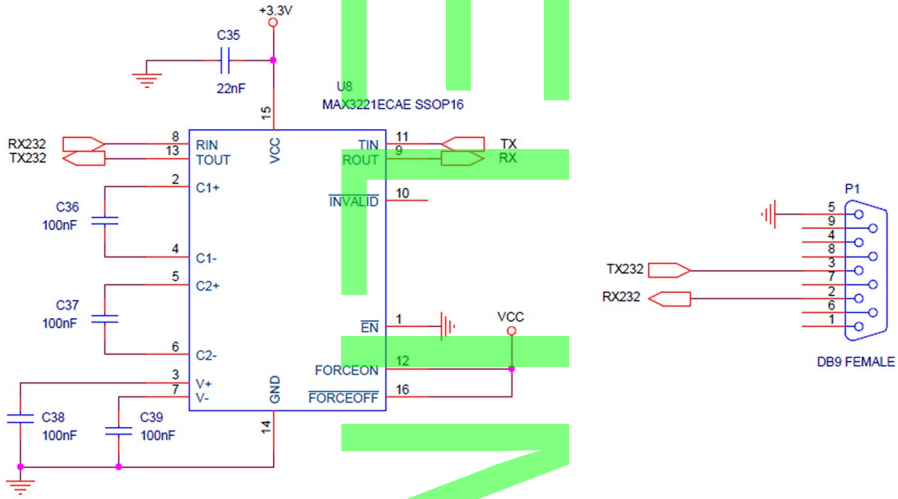
4.5. Serial interface

The **E663** features a serial communication for debugging and in case a custom firmware is running.

Observe the following schematic to implement this interface according to RS-232 specifications (+12V/-12V, DB9 plug).



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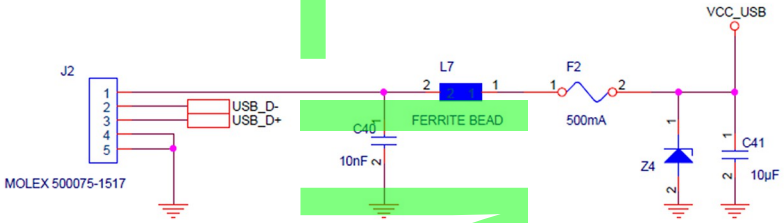
4.6. USB Interface

The USB interface is used for firmware upgrade only, i.e. it shall be used only when the /FLASH pin is tied to a 0 level.

All USB pins shall be left unconnected when the device is not in the firmware-upgrade mode.

4.6.1. Schematics

The **E663** features a USB 2.0 device interface. Observe the following schematics to implement this interface according to USB hardware specifications.

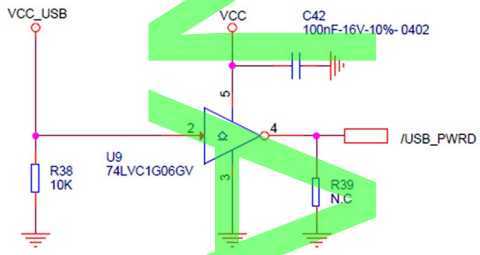


4.6.2. Powered by the bus, or external power

The /USB_PWRD pin (#14) tells the firmware whether the **E663** must be powered by the bus, or has another power supply (external power supply, or POE).

You must either tie the /USB_PWRD pin to the value depending on your hardware setup (LOW level if powered-by-the-bus, HIGH level if an external power supply is present).

Alternatively, you may also implement the following schematics to let the device detect automatically how it is powered:



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4.7. Firmware upgrade

The /FLASH pin (#10) is intended to put the **E663** in firmware upgrade mode. Set /FLASH to LOW and reset the module (or cycle power) to enter this mode.

The firmware upgrade is made through the USB interface. The **E663** must be flashed using **Renesas Flash Development Toolkit (FDT) version 4.09** and onwards. The CPU in the E663 is a Renesas RX62N. Please refer to the page "E663 firmware upgrade procedure" hosted on **SpringCard's developer blog** for details.

IMPORTANT DISCLAIMER:

DO NOT TRY TO UPGRADE THE FIRMWARE while the RF field is switched ON. To enter firmware upgrade mode safely, please either cycle power after setting the /FLASH pin to low, or switch RF field to OFF by sending appropriate software commands before any action on the /RESET pin.

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4.8. Recommended BOM

[To be written]

Component	Value	Tolerance	Recommended part #	Manufacturer

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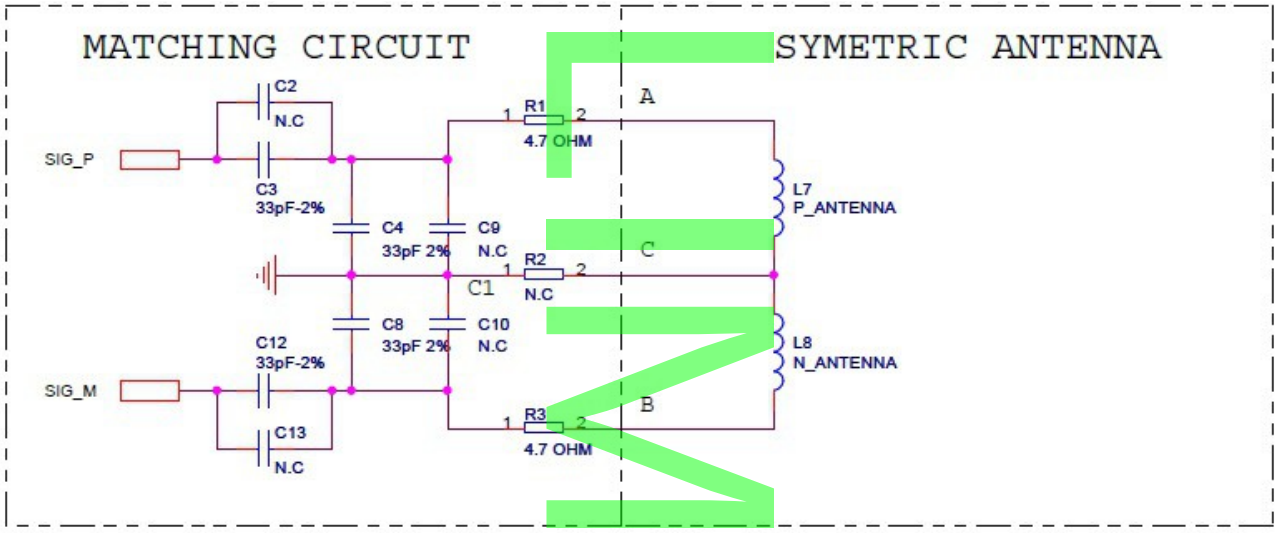
5. Symmetric (balanced) antenna (E663S)

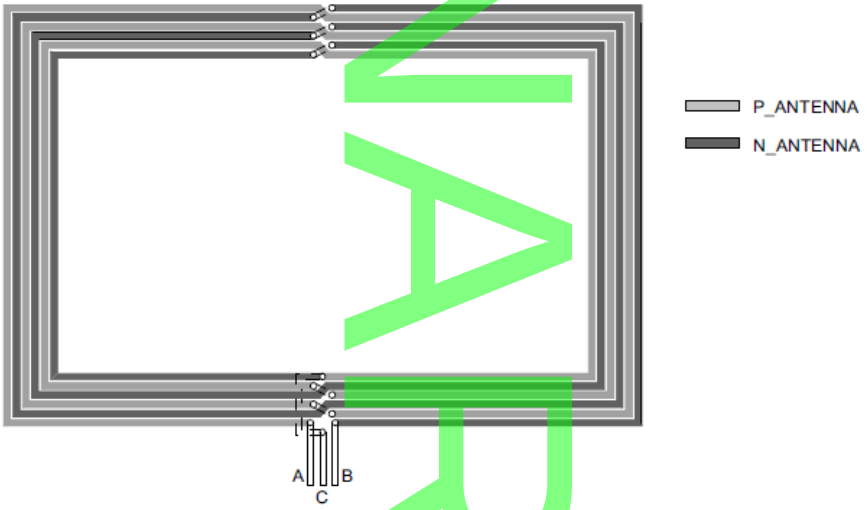
5.1. The SIG_P and SIG_M pins

E663's SIG_N pin (#1) and SIG_P pin (#2) are designed to drive a **balanced antenna.**

The antenna shall be connected to the module with 50mm maximum distance.



5.2. Antenna topology



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5.2.1. Shielding

This antenna does not need ground plane protecting against H field like Unbalanced Antenna (see 6.2.2).

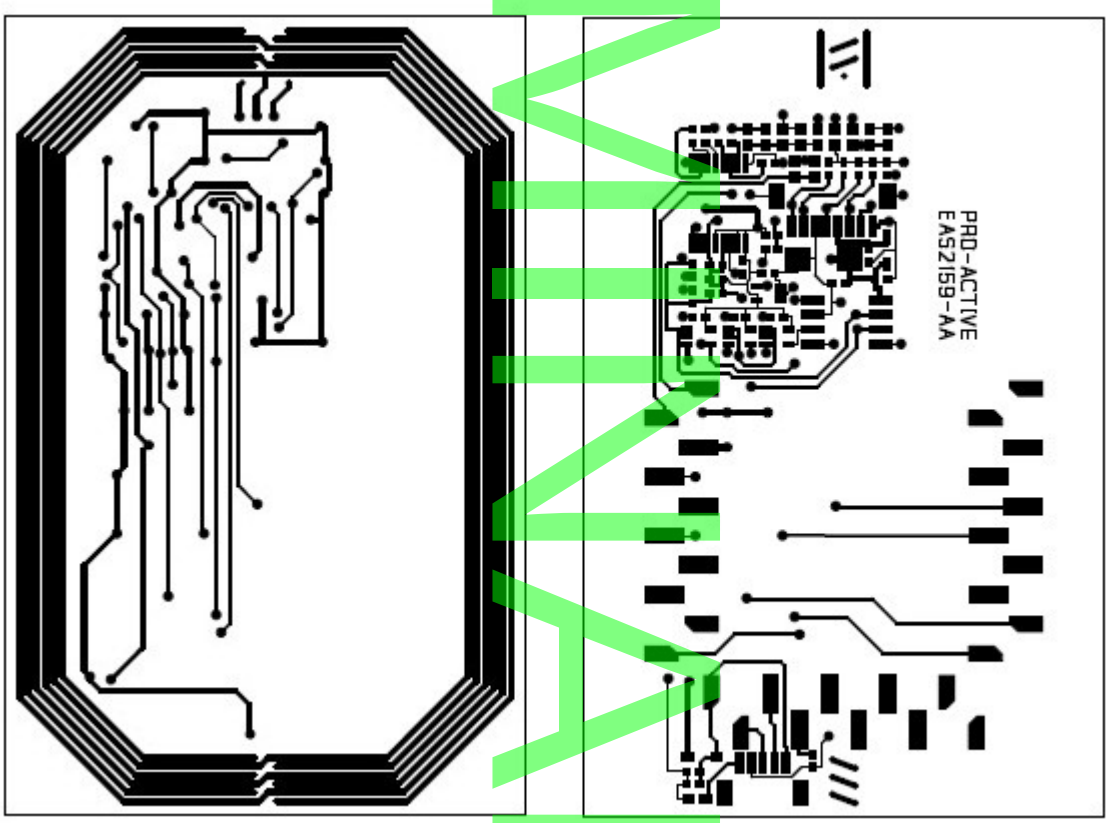
When P_Antenna has positive H field emission, the N_Antenna has an opposite H field emission, doing H fields vanish.

5.2.2. Matching and tuning circuit

This circuit has two roles:

- **Tune up** P_antenna and N_Antenna as a band-pass filter centred on 13.56MHz (C4, C9, C8, C10) with a **quality factor** (Q) of approx. 40 (R1, R3).
- **Match** P_antenna and N_Antenna to 100Ω (C2, C3, C12, C13).

5.3. Antenna reference



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5.4. Recommended BOM

Component	Value	Tolerance	Recommended part #	Manufacturer
C2, C9, C10, C13	*Unmounted*			
R2	*Unmounted*			
C3, C12	33pF/100V	2%	06031U270GAT2A	AVX
C4,C8	12pF/100V	2%	06031U150GAT2A	AVX
R94	4,7	5%	232273464708	PHYCOMP

5.5. Designing a custom antenna

Designing an antenna for 13.56MHz RFID or NFC applications requires expertise and can't be improvised. A poorly designed antenna may be the cause of a too-short operating distance, 'holes' in the operating volume, excessive power consumption and overheating, damages in the module's output stage, non-compliance with ISO standards and EMC regulations.

As reference documentations, please refer to NXP (formerly Philips Semiconductors) application notes on the subject:

- **NXP AN 077925 : Directly matched antenna design**
  http://www.nxp.com/documents/application_note/077925.pdf
- **NXP AN 78010 : 13.56MHz RFID proximity antennas**
  http://www.nxp.com/documents/application_note/78010.pdf

The RF chipset in H663 is NXP CLRC663. Please take into account RC663's limiting characteristics. **SpringCard** engineers have a strong experience in antenna design. Do not hesitate to consult us any time you need a custom design.

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Editor's information

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RCS EVRY B 429 665 482

Parc Gutenberg, 2 voie La Cardon

91120 Palaiseau – FRANCE

Contact information

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